

COMPUTER ARCHITECTURE AND ORGANIZATION (Common to CSE&IT)

II B. Tech. - I Semester
Course Code: A3CS06

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This course introduces the principles of computer organization and the basic architecture concepts. The course emphasizes performance and cost analysis, instruction set design, pipelining, memory technology, memory hierarchy, virtual memory management, and I/O systems. Basic technical writing skills are also taught in this class.

COURSE OBJECTIVES:

1. To impart basic concepts of computer architecture and organization,
2. To explain key skills of constructing cost-effective computer systems.
3. To familiarize the basic CPU organization.
4. To help students in understanding various memory devices.
5. To facilitate students in learning IO communication

COURSE OUTCOMES:

At the end of the course students will be able to:

1. Identify various components of computer and their interconnection
2. Identify basic components and design of the CPU: the ALU and control unit.
3. Compare and select various Memory devices as per requirement.
4. Compare various types of IO mapping techniques
5. Critique the performance issues of cache memory and virtual memory

SYLLABUS

UNIT - I

STRUCTURE OF COMPUTERS: Computer types, Functional units, Basic operational concepts, Von-Neumann Architecture, Bus Structures, Software, Performance, Multiprocessors and Multicomputer, Data representation, Fixed and Floating point, Error detection and correction codes.

COMPUTER ARITHMETIC: Addition and Subtraction, Multiplication and Division algorithms, Floating-point Arithmetic Operations, Decimal arithmetic operations.

UNIT - II

BASIC COMPUTER ORGANIZATION AND DESIGN: Instruction codes, Computer Registers, Computer Instructions and Instruction cycle. Timing and Control, Memory-Reference Instructions, Input-Output and interrupt. Central processing unit: Stack organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Complex Instruction Set Computer (CISC) Reduced Instruction Set Computer (RISC), CISC vs RISC

UNIT - III

REGISTER TRANSFER AND MICRO-OPERATIONS: Register Transfer Language, Register Transfer, Bus and Memory Transfers, Arithmetic Micro-Operations, Logic Micro-Operations, Shift Micro-Operations, Arithmetic logic shift unit.

MICRO-PROGRAMMED CONTROL: Control Memory, Address Sequencing, Micro-Program example, Design of Control Unit.

UNIT - IV

MEMORY SYSTEM: Memory Hierarchy, Semiconductor Memories, RAM(Random Access Memory), Read Only Memory (ROM), Types of ROM, Cache Memory, Performance considerations, Virtual memory, Paging, Secondary Storage, RAID.

UNIT – V

INPUT OUTPUT: I/O interface, Programmed IO, Memory Mapped IO, Interrupt Driven IO, DMA.

MULTIPROCESSORS: Characteristics of multiprocessors, Interconnection structures, Inter Processor Arbitration, Inter processor Communication and Synchronization, Cache Coherence.

TEXT BOOKS:

1. M. Moris Mano (2006), Computer System Architecture, 3rd edition, Pearson/PHI, India.

REFERENCE BOOKS:

1. Carl Hamacher, Zvonks Vranesic, SafeaZaky (2002), Computer Organization, 5th edition, McGraw Hill, New Delhi, India.
2. William Stallings (2010), Computer Organization and Architecture- designing for performance, 8th edition, Prentice Hall, New Jersey.
3. Anrew S. Tanenbaum (2006), Structured Computer Organization, 5th edition, Pearson Education Inc,
4. John P. Hayes (1998), Computer Architecture and Organization, 3rd edition, Tata McGrawHill