DIGITAL LOGIC DESIGN
(Common to CSE&IT)

II B. Tech. - I Semester	L	T	P	C
Course Code: A3EC19	3	1	-	3

COURSE OVERVIEW:

The course addresses the concepts, principles and techniques of designing digital systems.
The course teaches the fundamentals of digital systems applying the logic design and development techniques. This course forms the basis for the study of advanced subjects like Computer Architecture and Organization, Microprocessor through Interfacing, VLSI Designing. Students will learn principles of digital systems logic design.

COURSE OBJECTIVES:

1. To teach various number systems, binary codes and their applications
2. To familiarize the students the importance of error detection and error correction codes.
3. To inculcate concepts of K-MAP to simplify a Boolean expression
4. To facilitate students in designing a logic circuit

COURSE OUTCOMES:

At the end of the course students will be able to:

1. Use number systems and complements
2. Identify the importance of canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
3. Minimize functions using any type of minimizing algorithms (Boolean algebra, Karnaugh map or Tabulation method).
4. Analyze the design procedures of Combinational and Sequential circuits.
5. Design the finite state machine using algorithmic state machine charts and perform simple projects with a few flip-flops.

SYLLABUS

UNIT - I

DIGITAL SYSTEMS AND BINARY NUMBERS: Digital systems, binary numbers, number base conversions, octal and hexadecimal numbers, complements, signed binary numbers, binary codes, error detection and error correction codes.

BOOLEAN ALGEBRA AND LOGIC GATES: Basic definitions, axiomatic definition of Boolean algebra, basic theorems and properties of Boolean algebra, Boolean functions, canonical and standard forms, other logic operations, digital logic gates.

UNIT - II

GATE LEVEL MINIMIZATION: The k-map method, four-variable map, five-variable map, product of sums simplification, don't-care conditions, NAND and NOR implementation, determination and selection of Prime Implicants, Essential and Non essential prime Implicants.

UNIT - III

COMBINATIONAL CIRCUITS: Design procedure, Binary Adder, Binary Subtractor, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers, and Demultiplexers.

UNIT - IV

SYNCHRONOUS SEQUENTIAL LOGIC: Sequential circuits, latches, flip-flops, analysis of clocked sequential circuits, State reduction and assignment, design procedure.

REGISTERS AND COUNTERS: Registers, shift registers, ripple counters, synchronous counters, counters with unused states, ring counter, Johnson counter.

UNIT - V

MEMORY AND PROGRAMMABLE LOGIC: Introduction**,** Random access memory, memory decoding, error detection and correction, read only memory, programmable logic array, programmable array logic, sequential programmable devices.

TEXT BOOKS:

1. M. Morris Mano, Michael D. Ciletti (2008), Digital Design, 4th edition, Pearson Education Inc, India.

REFERENCE BOOKS:

1. Zvi. Kohavi (2004), Switching and Finite Automata Theory, Tata McGraw Hill, India.
2. C. V. S. Rao (2009), Switching and Logic Design, 3rd Edition, Pearson Education, India.
3. Donald D. Givone (2002), Digital Principles and Design, Tata McGraw Hill, India
4. Roth (2004), Fundamentals of Logic Design, 5th Edition, Thomson, India.